Govt. Polytechnic for Women at Rehan
Dairy No. 2127
Date 21/8/24
Distt. Kangra (H.P.)

Department of Computer Engineering
Govt. Polytechnic for Women Rehan
Distt. – Kangra (H.P.) - 176022

LESSON PLAN

Program Name	Computer Engineering
Subject Name	Computer System Architecture
Subject Code	COPC207& COPC217
Semester	Third
Subject Teacher Name	Madhulika

Evaluation Scheme

Sr. No.	Subject Name	Study scheme (Hrs/Week)		Marks in Evaluation Scheme					
				Internal Assessment			External Assessment		
		Th	Pr	Th	Pr	Total	Th	Pr	Total
1.	Computer System Architecture	2+01(DCS)	2	40	40	80	60	60	120
Reference Books		(i) Computer System Architecture, by M. Morris Mano.							
		(ii) Computer Organization and Architecture, William Stallings, Pearson							

Course Outcomes (COs)

CO – 1	Understand the basic building blocks of Computer System
CO – 2	Design combinational and sequential circuits
CO – 3	Understand the basic architecture and programming of a microprocessor (8085)
CO – 4	Demonstrate an understanding of the design of the functional units of a digital computer system
CO – 5	Explain Memory hierarchy of a computer system

Teaching Plan

Unit No.	Name of Topic	Proposed Date	Actual Date	Remarks
1	Functional units of Digital Computer, Computer Organization, Computer Design, Computer	01/08/2024 to 06/08/2024		
	Architecture, Von-Neumann and Harvard architecture, Bus Interconnection, Evolution of	07/08/2024 to 14/08/2024		
	Microprocessors, Concept of Microcomputer, Microcontroller and Embedded Systems.	20/08/2024 to 27/08/2024		
2	Number systems: Decimal, Binary, Octal and Hexadecimal. Conversion	28/08/2024 to		

	from one number system Signed Binary Numbers: Sign Magnitude Representation, One's	04/09/2024 05/09/2024 to 06/09/2024		
	Compliment Representation and Two's Compliment Representation. Binary Arithmetic:	09/09/2024 To 16/09/2024		
	Addition, Subtraction, Binary Arithmetic using one's and Two's Compliment. Fixed and Floating	17/09/2024 To 23/09/2024		
	Point Numbers, Computer Codes: BCD, EBCDIC, ASCII. Multiplication Algorithms - Hardware Implementation for Signed-Magnitude Data, Booth Multiplication Algorithm.	24/09/2024 To 30/09/2024		
3	Logic Gates: Symbols and Truth Table, Boolean Algebra, Logic Diagram, De Morgan's Theorem, Combinational Circuits: Block Diagram, Half Adder, Full Adder, Flip Flop: SR, D Flip	01/10/2024 To 08/10/2024		
	Flop and J K Flip Flop, Example of a sequential circuit, Decoder & Encoder: 3 to 8, Multiplexer De Multiplexer: 4 to 1 line.	09/10/2024 to 16/10/2024		
4	Basic features of 8085 Microprocessor, Block Diagram of 8085 Microprocessor, Functions of	16/10/2024 To 19/10/2024		
	various blocks, Concept of Buses, Bus Multiplexing and De-multiplexing, Status Flag	21/10/2024 To 23/10/2024		
	Addressing Modes and Interrupts.	24/10/2024		
5	Major Components of CPU, General Register Organization, Control Word, Stack Organization Register and Memory Stack. Reverse Polish Notation and Evaluation of Arithmetic Expressions;	25/10/2024 To 27/10/2024		
	Instruction formats – Three Address Instructions, Two Address Instructions, One Address	01/11/2024 To 05/11/2024		
	Instructions, Zero Address Instructions. Brief Introduction to RISC and CISC Processors, Concept of Parallel Processing and	06/11/2024 To 11/11/2024		

	Pipelining.			
6	Components of memory hierarchy: main memory, auxiliary memory and cache memory,	12/11/2024 To 16/11/2024		
	Introduction to Associative Memory, Cache Memory - Locality of Reference, Hit Ratio, Writing	18/11/2024 To 23/11/2024		
	into Cache - Write Through, Write Back, Input-Output Interface –Purpose, I/O Versus Memory Bus, Isolated versus Memory-Mapped I/O.	25/12/2024 To 02/12/2024		

Assignments

Assignment No	Contents of Syllabus Covered	Proposed Date	Actual Date	Remarks
A-1	Unit-1 and Unit-2	30-09-2024		
A-2	Unit-3 and Unit-4	24-10-2024		
A-3	Unit-5, Unit-6	25-11-2024		

House Test/Class Test

Name of test	Syllabus for Tests	Proposed Date	Actual Date	Remarks
Class Test -1	Unit-1 and Unit-2	As per HPTSB Academic Schedule		
Class Test -2	Unit-3 and Unit-4			
House Test - 1	Unit-1, Unit-2, Unit-3, Unit-4 and Unit-5			

Lab Plan

Sr. No.	Name of Practical	Proposed Date		Actual Date		Remarks
		G1	G2	G1	G2	
1	To study AND, OR, NOT logic gates and verify their truth tables (using breadboard)	03/08/2024	01/08/2024 08/08/2024			
2	To study NAND, NOR, Ex-OR logic gates and verify their truth tables (using breadboard)	17/08/2024	22/08/2024			
3	To realize basic gates (AND, OR, NOT) using NAND gates only	24/08/2024 31/08/2024	29/08/2024			
4	To realize basic gates (AND, OR, NOT) using NOR gates only	21/09/2024	05/09/2024 12/09/2024			
5	To realize DeMorgan's theorem.	28/09/2024	19/09/2024			
6	To design and implement Half adder &Full adder circuit.	05/10/2024	26/09/2024			
7	To design 7-segment decoder driver.	19/10/2024	03/10/2024			
8	To Verify the truth table of S-R	26/10/2024	10/10/2024			

	and JK flip flops.		24/10/2024			
9	To design and implement encoder and decoder.	16/11/2024	07/11/2024			
10	Addition and subtraction of two 8 bit numbers.	23/11/2024	14/11/2024			
11	To add two 8-bit numbers resulting in 16 bits sum.	23/11/2024	21/11/2024			
12	To find largest among two numbers.	30/11/2024	28/11/2024			
13	To sort a list of numbers.	30/11/2024	30/11/2024			

SGO Bhagwan 01/08/2024.
(Signature of Teacher)

11/8/2024
(Signature of HOD)

Approved

Principal
Govt. Polytechnic for Women Rehan